

AT  
Conceded  
457  
cont'd

3 p-channel typ MIS transistor and an n-channel type MIS  
4 transistor to which a substrate bias is applied in a reverse  
5 direction by the potential of said well region, and said  
6 second logic gate includes a p-channel type MIS transistor and  
7 an n-channel type MIS transistor to which a substrate bias is  
8 applied in a forward direction by a potential of said well  
9 region.

10. (Amended) A semiconductor integrated circuit  
according to claim 6, wherein said first logic gate includes a  
p-channel type MIS transistor to which a substrate bias is  
applied in a reverse direction by a potential of said well  
region, and said second logic gate includes a p-channel type  
MIS transistor to which a substrate bias is applied in a  
forward direction by a potential in said well region.

11. (Amended) A semiconductor integrated circuit  
according to claim 6, wherein said first logic gate includes a  
p-channel type MIS transistor and an n-channel type MIS  
transistor to which a substrate bias is applied in a reverse  
direction by a potential in said well region.

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Please add the following new claims:

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A<sub>2</sub>

39. (New) A semiconductor integrated circuit according  
to claim 7, wherein said first logic gate includes an MIS  
transistor to which a substrate bias is applied in a reverse

direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

40. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

41. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

42. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to